

Advanced Interconnect Technology in the era of Heterogenous Integration

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[Abstract]

As the pace of the conventional semiconductor scaling slows down due to the mounting challenges arising from the nanometer scale feature sizes, the industry is seeking for breakthroughs to continue PPA (power, performance, area) improvement from the 3D-integration of the chip level and advanced packaging of multiple heterogenous integrated semiconductor dies. The conventional BEOL interconnect is also benefited by this industry trend of three-dimensional integration with disaggregation while it continues to address various challenges in RC delay reduction and reliability associated with pitch scaling. For instance, the backside of a wafer became accessible thanks to wafer bonding and thinning technology and the BSPDN (backside power distribution network) is being investigated actively by the industry. When the power rails are separated from the signal lines and moved to wafer backside, significant benefits in design efficiency and device performance can be achieved. In this talk, various aspects of the BSPDN scheme will be discussed in conjunction with the conventional scaling technologies for frontside interconnect. 3D integration of the functionality elements to BEOL such as embedded memories and innovative switching devices is the other important approach to reduce footprint and increase the computing speed especially for AI (artificial intelligence) applications.

Continued innovations in BEOL scaling, backside processing and functional BEOL elements will be implemented either collectively or complementarily to meet the demands for advanced devices and systems. For future devices beyond conventional CMOS, we need to expand the concept of the interconnect as an active building block for the advanced packaging and 3D integration because the improved performance and built-in flexibility in each chip will eventually provide freedom to the overall system design optimization.

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